

## CLAIMS

1. Miniaturized temperature-zone flow reactor comprising at least one  
multifold wound flow path, formed in a plane substrate by  
microstructurized channels, characterized in that each of said flow  
paths constituting a closed flow path is subdivided into at least  
three partial paths (A1...An; B1...Bn, and BB1...BBn-1; C1...Cn) in  
such a way that three substrate chips (A; B; C), made of a material  
of a thermal conductivity as high as possible, are provided,  
whereby the substrate chips on one of their faces are, at least on  
those ranges being provided with channels, entirely and level  
captured by a heating means (H), which permits application of a  
controllable and variable temperature, and in that  
the first substrate chip (A) is provided with inlets (az1), the number  
of which corresponds to the number of the flow paths present, and  
that a third substrate chip (C) is provided with outlets (ca4), the  
number of which corresponds to the number of the flow paths  
present, and said substrate chips (A;C) are each provided with n  
channel sections, each of said n channel sections having an inlet  
opening and an outlet opening (az1...aa4; cz1...ca4) which are  
arranged on one side substantially along a line side by side on a  
partial section of the respective substrate chip,  
that the first substrate chip (A) and the third substrate chip C being  
spaced apart from one another are arranged via that surface, which  
is opposite to the heating means (H), on a first face (V1) of a  
connecting chip (V), which, being of poor thermal conductivity, is

provided with passage openings (Vd), above said connecting chip (V), and connected to the latter in such a manner that said inlet openings (aa1...aa4) and said outlet openings (cz1...cz4) are captured by said passage openings (Vd), said passage openings (Vd) being connected with one another on the second face (V2) of said connecting chip (V) via microstructurized channels, which form the partial paths (B1...Bn, and BB1...BBn-1) of the second substrate chip (B), whereby one closed flow path each with n passages through the substrate chips (A; B; C) is constituted.

2. Miniaturized temperature-zone flow reactor as claimed in claim 1, characterized in that the respective return channels (BB1...BBn-1) of the partial paths (B1...Bn, and BB1...BBn-1) of the second substrate chip (B) are given a reduced flow cross-section compared to the remaining n channels (B1...Bn) in such a way, that the speed of passage flow through the return channels (BB1...BBn-1) is at least increased by the threefold relative to the speed of passage flow through the remaining channels (B1...Bn).

3. Miniaturized temperature-zone flow reactor as claimed in claim 1 <sup>or</sup> and 2, characterized in that the channels formed by the return channels (BB1...BBn-1) are provided with a thermally insulating lining relative to the substrate chip (B).

4. Miniaturized temperature-zone flow reactor as claimed in claim 3,  
characterized in that the thermally insulating lining is constituted  
by a polymer.
- 5 5. Miniaturized temperature-zone flow reactor as claimed in claim~~s~~ 1  
<sup>or</sup>  
~~and~~ 2, characterized in that the connecting chip (V) is made of an  
optically transparent material.
- 10 6. Miniaturized temperature-zone flow reactor as claimed in claim 1,  
characterized in that the first inlet path (az1 to aa1) in the first  
substrate chip (A) and the last outlet path (cz4 to ca4) in the third  
substrate chip (B) are designed longer than the remaining n partial  
channels provided on the respective substrate chips.
- 15 7. Miniaturized temperature-zone flow reactor as claimed in claim 1,  
characterized in that a liquid non-mixable with the sample, in  
particular oil, is used as a carrier medium for the sample transport.
- 20 8. Miniaturized temperature-zone flow reactor as claimed in claim 1,  
characterized in that the second substrate chip (B) on one side is  
captured by a level cooling means (K) to generate a reduced  
temperature compared to the temperature reduced by the remaining  
substrate chips (A, B).